FLIP CHIP PROCESS

CROSS-REFERENCE TO RELATED APPLICATION

This application claims the priority benefit of Taiwan application serial no. 89127631, filed December 22, 2000.

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] The present invention relates to a flip chip process. More particularly, the present invention relates to a wafer level flip chip packaging process.

Description of the Related Art

[0002] As the era of information technology progresses, the transmission and processing of information and documents are extensively accomplished by means of electronic products. Accompanying the progress of technology, many commercial products with more convenient features are promoted, as mobile phones, computers, audio-video articles, while the emphasis is made to miniaturization.

[0003] In this present context, integrated circuit packaging processes, accompanying the development of integrated circuit manufacturing, emphasizes on high density products. Consequently, many high pin-count packaging structures and high-density chip scale packaging (CSP) structures are developed. Flip chip technology is extensively employed in chip scale packaging (CSP). "Flip chip" principle consists of mounting and connecting directly the chip to the carrier via a plurality of bumps, which

advantageously shortens the electrical path and reduces the surface area of the package. In order to improve the throughput and simplify the packaging processes, wafer-level packaging is also extensively developed. Used in wafer-level packaging, flip chip technology can substantially improve the throughput and the efficiency of the packaging processes and reduce the manufacturing time.

[0004] Referring to FIG. 1 and FIG. 2, cross-sectional views schematically illustrate a conventional flip chip packaging process. As shown in FIG. 1, in the conventional flip chip packaging process, a surface 102 of a chip 100 is conventionally provided with a plurality of bonding pads 104. A bump 106 is formed on each bonding pad 104. A surface 152 of a substrate 150 is provided with a plurality of contact pads 154, wherein each of the contact pads 154 respectively corresponds to each of the bonding pads 104 of the chip 100. The bumps 106 of the chip 100 are aligned and put in contact with the contact pads 154 of the substrate 150. A reflow process then is performed to connect the chip 100 to the substrate 150 via the bumps 106. After reflow process, the reflowed bumps 106 are referred to as a plurality of connecting bumps 108 that connects the chip 100 to the substrate 150. An underfill material 180 is filled between the chip 100 and the substrate 150, wherein the underfill material 180 encapsulates the connecting bumps 108. The underfill material 180 then is solidified.

[0005] In the above conventional flip chip process, the wafer on which are formed the chips 100 usually has to be diced to obtain individualized chips. Then, each of the chips 100 is flipped such that the bumps 106 are downside to connect onto the substrate. Such a conventional process is substantially time-consuming, reduces the throughput and lowers the efficiency of the packaging process.

SUMMARY OF THE INVENTION

[0006] An aspect of the present invention therefore is to provide a flip chip packaging process that can substantially improve the throughput and the efficiency of the production.

[0007] To attain at least the foregoing objectives, the present invention provides a flip chip packaging process that comprises the following steps. A wafer is provided with a plurality of chips, wherein an active surface of each chip has a plurality of bonding pads. A plurality of bumps are respectively formed on the bonding pads of the chips. A plurality of substrates respectively include at least a package unit therein, wherein each package unit further includes a plurality of contact pads. The substrates are respectively mounted on the wafer such that each package unit corresponds to one chip and the contact pads of the package unit are respectively connected to the bumps attached to the chip. Mounted onto the wafer, two neighboring substrates are separated by a gap. An underfill material is introduced through the gaps between the substrates and from the boundary of the wafer to fill the space between the wafer and the substrates. The underfill material then is solidified. A dicing process is performed to separate the chips and package units of the substrates into a plurality of individual flip chip packages.

[0008] To attain at least the above objectives, the present invention, according to another embodiment, provides a flip chip process that comprises the following steps. A wafer is provided with a plurality of chips therein, wherein an active surface of each chip comprises a plurality of bonding pads thereon. A plurality of substrates further respectively include at least a package unit, wherein the surface of each package unit includes a plurality of contact pads thereon. A bump is respectively formed the

contact pads of the package units. The substrates are respectively mounted onto the wafer such that each package unit corresponds to one chip and the bumps attached to the package unit are respectively connected to the bonding pads of the chip. Mounted on the wafer, two neighboring substrates are separated by a gap. An underfill material is introduced through the gaps between the substrates and from the boundary of the wafer to fill the space between the wafer and the substrates. The underfill material then is solidified. A dicing process is performed to separate the chips and package units of the substrates into a plurality of individual flip chip packages.

[0009] The substrate includes, for example, at least a patterned conductive layer laminated with at least an insulating layer. The surface of each package unit is smaller or equal to the surface of the corresponding chip.

[0010] It is to be understood that both the foregoing general description and the following detailed description are exemplary, and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention. In the drawings,

[0012] FIG. 1 and FIG. 2 are cross-sectional views illustrating the conventional flip chip packaging process;

[0013] FIG. 3, FIG. 4 and FIG. 5 are cross-sectional views showing different stages in a flip chip packaging process according to an embodiment of the invention;

[0014] FIG. 6 is a cross-sectional view illustrating a flip chip packaging process according to a second embodiment of the invention; and

[0015] FIG. 7 is a cross-sectional view showing an alternative example of the flip chip packaging process of the invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0016] The features and advantages of the present invention will be more clearly understood from the following detailed description taken in conjunction with the accompanying drawings. The following detailed description is only illustrative and not limiting.

[0017] Referring now to FIG. 3 to FIG. 5, various cross-sectional views schematically illustrate various stages in a flip chip packaging process according to a first embodiment of the invention. A wafer 200 is provided with a plurality of chips 210 and a plurality of wafer scribe lines 202 thereon. The wafer scribe lines 202 space apart the chips 210 from one another. An active surface 212 of each chip 210 includes a plurality of bonding pads 214 thereon. A bump 216 is respectively formed on the bonding pads 214 of the chips 210. The bumps 216 are made of conductive material such as tin-lead alloy, gold or conductive polymer, for example.

[0018] A plurality of substrates 250 are provided with at least a package unit 270 therein. The substrates 250 can be fabricated from, for example, a plurality of patterned conductive layers 254 alternately laminated with insulating layers 256. The insulating layer 256 can be made of, for example, FR-4, FR-5, bismaleimide-triazine (BT), polyimide, epoxy, or ceramic. Alternately, the substrates 250 can be a single-layer substrate comprising a single patterned conductive layer and a single insulating

layer. In the present description, the substrates 250 are described as exemplary multi-layer substrates.

[0019] The package units 270 are spaced apart from one another by a plurality of substrate scribe lines 252. Each package unit 270 has a front surface 260 and a back surface 258. A plurality of contact pads 272 are formed on the back surface 258 and a plurality of outward contact pads 274 are formed on the front surface 260 of each package unit 270. A plurality of through holes 262 formed in the insulating layer 256 of each package unit 270 are filled with a conductive material 264 such that the contact pads 272 are respectively connected to the outward contact pads 274 through the vias (262+264) thus formed. The substrates 250 are disposed above the wafer 200, wherein the back surface 258 of the package units 270 is smaller or equal to the surface 212 of the chips 210.

[0020] Referring to FIG. 3 and FIG. 4, cross-sectional views schematically illustrate the electrical connection process. The substrates 250 are respectively mounted onto the wafer 200 such that the contact pads 272 of each package unit 270 are respectively aligned and in contact with the bumps 216 attached to each chip 210, wherein a gap 278 separates two neighboring substrates 250. A reflow process then is performed to connect the package units 270 to the chips 210. Reference numeral 218 now refers to a plurality of connecting bumps after the bumps 216 are reflowed. After the reflowing process, flux residues (not shown) conventionally used during the reflowing may remain on the active surface 212 of the chips 210. Solvents thus are conventionally used to clean the active surface 212.

[0021] Once the substrates 250 are arranged on the chips 210, the space between the wafer 200 and the substrates 250 are filled with an underfill material 290

introduced through the gaps 278 between the substrates 250 and from the boundary of the wafer 200. The underfill material 290 can be introduced under liquid form, for example, to obtain uniform distribution and prevent air voids, and subsequently solidified through a thermal process. The thus formed underfill material 290 encapsulates the connecting bumps 218. Reference numeral 292 represents the profile extension of substrate scribe lines 252 in the underfill material 290.

[0022] Referring to FIG. 4 and FIG. 5, the wafer 200 and substrates 250 are diced through the scribe lines 202, 252 and 292 to singularize and form individualized flip chip packages.

[0023] A plurality of solder balls 280 are respectively formed on the outward contact pads 274 of the package units 270. The solder balls 280 provide the individual flip chip packages with electrical connection to external devices.

[0024] As described above with reference to FIG. 3 through FIG. 5, the package units 270 are formed in specifically designed substrates 250. Thus, all the package units 270 can be simultaneously arranged onto the chips 210 to connect the bonding pads 214 of the chips to the contact pads 272 of the package units 270 through the bumps. The substrates 250 and the wafer 200 mounted to each other then can be diced to form the individual flip chip packages. The time of processing thus can be shortened and the throughput improved. Moreover, the surface of the substrates 250 is relatively small in the invention such that the underfill material 290 can be uniformly filled, and the mounting of the wafer 200 and the substrates 250 can be facilitated. As a result, the workability and efficiency of the flip chip process are improved.

[0025] In the previous description of the invention, the bumps are formed on the bonding pads of the chips. However, the bumps 402 can be first formed on the

contact pads 272 of the package units 270 as shown in FIG. 6. A reflow process then is performed with the bumps 402 attached to the package units 270 and put in contact with the bonding pads of the chips.

[0026] In the previous description of the present invention, a plurality of package units are integrated in a single substrate. However, each substrate 500 can have, for example, a single package unit 510 therein, wherein the back surface 512 of the package unit 510 is smaller than the active surface 212 of the corresponding chip 210, as shown in FIG. 7.

[0027] In conclusion, the foregoing description of embodiments and examples of the present invention reveals at least the following advantages. Since the package units, integrated into a plurality of substrates, are simultaneously bonded and connected to the chips and, subsequently, the substrates and the wafer are together singly diced, the time of processing thus can be shortened and the throughput improved. Moreover, the wafer-level packaging of the present invention uses a plurality of substrates that respectively include a plurality of package units, which differs from the conventional wafer-level packaging method in which a single substrate is bonded and connected to a single chip. As a result, the efficiency of the wafer-level packaging process can be substantially improved, and the filling of the underfill material, problematic in the prior art, can be made more workable and efficient.

[0028] It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the present invention without departing from the scope or spirit of the invention. In view of the foregoing, it is intended that the present invention cover modifications and variations of this invention provided they fall within the scope of the following claims and their equivalents.